

Amendments to the Claims:

Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Please amend claims 1, 3, 4, 20, 22, 23 and 25 as set forth hereinbelow.

Listing of Claims:

1. (Currently Amended) A method of forming an integrated circuit package, the method comprising:
forming a lead frame having a plurality of ~~conductors~~ leads and at least one alignment feature distinct from the plurality of leads and configuring the at least one alignment feature for cooperative engagement with a structure external to the integrated circuit package;
coupling at least some of the plurality of ~~conductors~~ leads to a semiconductor die;
encapsulating the semiconductor die and a portion of the lead frame with an insulating material;
electrically isolating the at least one alignment feature from the plurality of ~~conductors~~ leads subsequent the encapsulating the semiconductor die and a portion of the leadframe while maintaining the at least one alignment feature as a part of the integrated circuit package;
and
removing the at least one alignment feature subsequent the electrically isolating the at least one alignment feature from the plurality of ~~conductors~~ leads.

2. (Canceled)

3. (Currently Amended) A method of forming an integrated circuit package, the method comprising:
forming a leadframe having a plurality of ~~conductors~~ leads and at least one alignment feature distinct from the plurality of leads and configuring the at least one alignment feature for cooperative engagement with a structure external to the integrated circuit package;

coupling at least some of the plurality of ~~conductors~~ leads to a semiconductor die; and encompassing the semiconductor die, a portion of each of the plurality of ~~conductors~~ leads, and substantially encompassing the at least one alignment feature with an insulating material; and electrically isolating the at least one alignment feature from the plurality of ~~conductors~~ leads while maintaining the at least one alignment feature as a part of the integrated circuit package.

4. (Currently Amended) A method of forming and testing an integrated circuit package, the method comprising:
forming a leadframe having a plurality of ~~conductors~~ leads and at least one alignment feature distinct from the plurality of leads;
electrically coupling at least some of the plurality of ~~conductors~~ leads to a semiconductor die; encompassing the semiconductor die, a portion of each of the plurality of ~~conductors~~ leads, and substantially encompassing the at least one alignment feature with an insulating material; electrically isolating the at least one alignment feature from the plurality of ~~conductors~~ while maintaining the at least one alignment feature as a part of the integrated circuit package; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and testing the integrated circuit package through at least some of the electrically coupled conductors.

5-17. (Canceled)

18. (Original) The method according to claim 1, further comprising forming the at least one alignment feature to include at least one aperture.

19. (Original) The method according to claim 1, further comprising forming the at least one alignment feature to include a plurality of apertures.

20. (Currently Amended) The method according to claim 1, further comprising forming a separation line in the lead frame prior to removal of the at least one alignment feature and wherein removing the at least one alignment feature further comprises removing the at least one alignment feature along the separation line.

21. (Original) The method according to claim 20, wherein the forming a separation line in the lead frame includes perforating the separation line.

22. (Currently Amended) The method according to claim 1, further comprising forming the at least one alignment feature to include a tab protruding from an outer peripheral boundary of the insulating material.

23. (Currently Amended) A method of forming and testing an integrated circuit package, the method comprising:
forming a lead frame having a plurality of ~~conductors~~ leads and at least one alignment feature distinct from the plurality of leads;
coupling at least some of the plurality of ~~conductors~~ leads to a semiconductor die;
encapsulating the semiconductor die and a portion of the lead frame with an insulating material;
electrically isolating the at least one alignment feature from the plurality of ~~conductors~~ leads subsequent the encapsulating the semiconductor die and a portion of the lead frame with an insulating material while maintaining the at least one alignment feature as a part of the integrated circuit;
coupling the at least one alignment feature with a portion of a testing device;
testing the integrated circuit package through at least some of the electrically coupled ~~conductors~~ leads;
decoupling the at least one alignment feature from the portion of the testing device; and
removing the at least one alignment feature subsequent the decoupling the at least one alignment feature from the portion of the testing device.

24. (Original) The method according to claim 3, further comprising forming the at least one alignment feature to include an alignment cut-out.

25. (Currently Amended) The method according to claim 3, further comprising disposing a heat spreader adjacent to, and in contact with, an external surface of the insulating material ~~and~~, forming at least one other alignment feature in the heat spreader and configuring the at least one other alignment feature to substantially correspond in size and shape to the at least one alignment feature such that the at least one alignment feature and the at least one other form a cooperative alignment structure.

26. (Original) The method according to claim 3, further comprising providing a tie bar and forming the at least one alignment feature in the tie bar.